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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/191,708 | 11/13/1998 | BRIJ BHUSHAN GARG | L0012/7004 | 8933 |

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| EXAMINER |
|---|
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| ART UNIT | PAPER NUMBER |
|---|---|
| 2662 | |

DATE MAILED: 02/25/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/191,708 | GARG ET AL. | |
| | Examiner | Art Unit | |
| | Joe Logsdon | 2662 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *29 January 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

## Objections:

1. The amendment filed 29 January 2002 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: "A physical embodiment for the input and output bit maps may be realized by ... of the illustrative embodiment." This sentence was apparently introduced to obviate the last paragraph of the enablement rejection and therefore constitutes new matter.

Applicant is required to cancel the new matter in the reply to this Office Action.

## Claim Rejections—35 U.S.C. 112, First Paragraph:

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-22 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claims 1, 5, 6, 11, 16, and 20 use the term "time slot." The specification fails to define "time slot" as it relates to the claimed invention. For example, consider Fig. 7, which is discussed

on pages 12 and 13 of the specification. In Fig. 7, it is stated in parentheses, "One time slot at a time." The significance, and indeed meaning, of "time slot" is unclear; one may guess that 32 bits arrive in each "time slot" or that 32 bytes arrive in each "time slot." In this case perhaps 32 multiplexers are active in each of the 24 time slots; in the former case each multiplexer selects one bit per time slot, and in the latter case each multiplexer selects a string of 8 bits per time slot. One may instead guess that only one bit arrives in each "time slot" on the 32-bit bus. In this case perhaps only one multiplexer is active in each time slot. One of ordinary skill in the art would have no way of determining the number of time slots that are being used for any specific embodiment. The specification therefore fails to enable one of ordinary skill in the art to make or use the invention as claimed.

Furthermore, the apparatus and its method of use, as described in claims 1, 5, 6, 11, 16, and 20, is sufficiently complex that a reasonably detailed description, including a set of detailed drawings, is necessary to enable one of ordinary skill in the art to make or use the invention as claimed. According to Van Hoogenbemt, the selector circuitry is very complex (column 1, lines 21-25; column 1, lines 35-40). The selector circuitry depicted as 701 in Fig. 7 lacks enabling detail because it fails to teach a design of the selector that would allow the selector to perform its intended function. As described on pages 5 and 6 of the specification, the figures only provide functional level block diagrams of the claimed invention. The specification therefore fails to enable one of ordinary skill in the art to make or use the invention as claimed.

Claims 2-4, 7-10, 12-15, 17-19, 21, and 22 depend on claims 1, 5, 6, 11, 16, and 20 and are therefore similarly rejected.

Furthermore, claims 7, 8, 12, and 13 describe "bit maps." Although the specification states, on page 11, lines 22-27, that input and output data bits can be represented by a matrix referred to as a bit map, as depicted in Fig. 6, the specification nowhere offers a physical embodiment for the bit maps. The specification provides no working example and no explanation that might enable one of ordinary skill in the art to make or use the invention as claimed.

## Claim Rejections—35 U.S.C. 102(b):

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Tocci. Tocci teaches a demultiplexer, which corresponds to the case where N=T=M=T2, R2=4, and R=1 (pages 388-394). As defined in the specification, "rails" in the claims can be "lines" as used in Tocci. There is a plurality of inputs (DATA input and SELECT inputs; Fig. 9.28). There is one data input, Z, so R=1 (Fig. 9.33 on page 393). An example is depicted in which 16 input positions (N=16), corresponding to 16 time slots (T=16), are switched to 16 output positions (M=16) ($A_0$-$A_3$, $B_0$-$B_3$, $C_0$-$C_3$, and $D_0$-$D_3$) arranged as 16 time slots (T2=16) on 4 rails (R2=4) ($O_0$-$O_3$) (Fig. 9.33 on page 393). Input data are arranged as bit packs, which can be bits according to the specification, in 16 time slots on 1 rail; data from the rail are selected and sent to the

output (pages 391-394). The output has 16 positions and 4 rails (Fig. 9.32; Fig. 9.33; pages 392-393).

## Claim Rejections—35 U.S.C. 103(a):

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 6, 11, and 16-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Hoogenbemt.

With regard to claims 6 and 20-22, Van Hoogenbemt discloses an interfacing device that extracts M outgoing sets of bits (bit packs) out of N incoming sets of bits (abstract). According to

one embodiment there are M multiplexers in the interfacing device; each multiplexer (a selection block) selects one of its N-M+1 inputs to place at the output (column 2, lines 37-45). Although Van Hoogenbemt does not explicitly state the number of time slots or the number of input or output rails, the interfacing device inherently uses some number, T, of time slots for the input; some number, T2, of time slots for the output; some number, R, of input rails; and some number, R2, of output rails. Van Hoogenbemt fails to teach that the number of inputs to each multiplexer is the same as the number of input rails. It would have been obvious to one of ordinary skill in the art to modify the invention of Van Hoogenbemt so that the number of inputs to each multiplexer is the same as the number of input rails because through appropriate modification of the selection inputs to the multiplexers any combination of inputs could be output from the set of multiplexers, and any change in strategy could easily be implemented through modification of software that controls the selection inputs.

With regard to claims 11 and 16-19, Van Hoogenbemt discloses an interfacing device that extracts M outgoing sets of bits (bit packs) out of N incoming sets of bits (abstract). According to one embodiment there are M multiplexers in the interfacing device; each multiplexer (a selection block) selects one of its N-M+1 inputs to place at the output (column 2, lines 37-45). Although Van Hoogenbemt does not explicitly state the number of time slots or the number of input or output rails, the interfacing device inherently uses some number, T, of time slots for the input; some number, T2, of time slots for the output; some number, R, of input rails; and some number, R2, of output rails. Van Hoogenbemt fails to teach that the number of inputs to each multiplexer is the same as the number of input positions and that the number of multiplexers is the same as the number of output data rails. It would have been obvious to one of

ordinary skill in the art to modify the invention of Van Hoogenbemt so that the number of inputs to each multiplexer is the same as the number of input positions to the interface device, and the number of multiplexers is the same as the number of output data rails, because through appropriate modification of the selection inputs to the multiplexers any combination of inputs could be output from the set of multiplexers, and any change in strategy could easily be implemented through modification of software that controls the selection inputs.

## Response to Arguments:

9. Applicant argues that Tocci does not anticipate the claims because Tocci teaches only one input. Applicant maintains that the preamble of the claims, which for claim 1 recites, "Apparatus for switching data from any of a plurality of inputs to any of a plurality of outputs". limits the claims to apparatuses comprising more than one input. But this quoted preamble in no way suggests that the apparatus comprises more than one input. The preamble merely specifies that the apparatus has a certain purpose, i.e., for switching data from any of a plurality of inputs (inputs to an apparatus which is not necessarily the claimed apparatus) to any of a plurality of outputs (outputs from an apparatus which is not necessarily the claimed apparatus). Furthermore, the demultiplexer in Tocci indeed has several inputs. It has one DATA input and several SELECT inputs (see Fig. 9.28). The demultiplexer switches data from one of the several inputs (i.e., DATA input) to any of a plurality of outputs. Any of the SELECT inputs could clearly be substituted for the DATA input. Therefore, data from any of the plurality of inputs could be

switched to any of the plurality of outputs. This Office Action has been modified to make this point clear. This is not, however, a new grounds for rejection.

Applicant notes that Tocci fails to teach several input data lines. But the claims likewise fail to teach this element, as explained above.

Applicant argues that the claims should not be rejected under 35 U.S.C. 103(a) because for the invention of Van Hoogenbemt to switch data from any of N input positions to any of M output positions the interconnections of the logical cells constituting the matrix in CTRL would have to be rearranged. But the claims in no way suggest that such rearrangement is unnecessary for altering the relative order between input and output. Furthermore, the use of appropriate logic circuits to effect the rearrangement noted by Van Hoogenbemt would have been obvious to one of ordinary skill in the art.

With regard to the enablement rejections, it is impossible for data from any of N input positions arranged as T time slots on R rails to be switched to any of M output positions arranged as T2 time slots on R2 rails without some type of constraint that relates these parameters. If a "time slot" has the same duration at the input to the switch as it does at the output from the switch, then on average the same number of bits must appear in each time slot at the input to the switch as at the output from the switch—unless bits are added or dropped from the apparatus, which the specification does not teach. Even if bits were added or dropped, it would still not be possible for data from any of N input positions arranged as T time slots on R rails to be switched to any of M output positions arranged as T2 time slots on R2 rails. Apparently, the meaning of "time slot" at the input differs from that at the output.

Applicant states that "The time slots are defined by the number of bits switched within a single time slot." This circular definition does not define "time slot."

Applicant objects to the use of Van Hoogenbemt to support the enablement rejection. According to Applicant, Van Hoogenbemt's statement that "the selector circuitry is very complex" is irrelevant. The complexity of the art is, however, a relevant consideration for any enablement rejection. If one of extraordinary skill in the art, e.g., an inventor, states that the selector circuitry is very complex, then it must be—in the inventor's opinion—at least very complex to one of ordinary skill in the art. Of course, the quoted statement is an expression of opinion, but it is a relevant factor. (see MPEP §2164.01(a))

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lee is cited to show the state of the art.

## Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Logsdon whose telephone number is (703) 305-2419. The examiner can normally be reached on Monday through Friday from 1:00 pm to 9:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou, can be reached at (703) 305-4744.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-4700.

13. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

**Or faxed to:**

(703) 872-9314

For informal or draft communications, please label "PROPOSED" or "DRAFT".

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Joe Logsdon

Patent Examiner

Friday, February 15, 2002

HASSAN KIZOU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600